What Is Claimed Is:

1. A method for error detection in a cache memory for storing data, the access to the data stored in the cache memory taking place by addresses assigned to them,
wherein for the addresses assigned to the stored data, at least one first test signature made up of at least one first signature bit is generated and also stored in the cache memory.

2. The method as recited in Claim 1,
wherein a checking of the first test signature takes place for each read access to the cache memory.

3. The method as recited in Claim 1,
wherein, the at least one stored first signature bit of the first test signature is compared to a second signature bit of a second test signature, which is formed from an address applied at the cache memory.

4. The method as recited in Claim 1,
wherein the at least one stored first signature bit of the first test signature is compared to a second signature bit of a second test signature, which is transferred together with an address applied at the cache memory.

5. The method as recited in Claim 1,
wherein a valid-invalid bit is stored at least in duplicate in the cache memory.

6. The method as recited in Claim 5,
wherein the valid-invalid bit is stored m-fold and is checked using an n of m test, m, n being natural numbers and m being > 2 and m>n>m/2.

7. The method as recited in Claim 5,
wherein the valid-invalid bit is stored k-fold as a bit combination in the form of a 1 of k code, by comparison 1 bit combination of 2^k bit combinations being detected as valid, k corresponding to a natural number.

8. The method as recited in Claim 1,
wherein the data are made up only of instructions.

9. The method as recited in Claim 1,
wherein to a group of data and the appertaining first test signatures, in each case a first line index is assigned in the cache memory, and this is compared to a second line index applied at the cache memory, this first line index being retrieved from the cache memory by line decoding.

10. The method as recited in Claim 3 or 4 or 5 or 6 or 7 or 9,
wherein an error signal is generated as a function of the respective comparison result.

11. The method as recited in Claim 10,
wherein the error signal is treated as a cache miss signal.

12. The method as recited in one of Claims 2 through 9,
wherein at least one error is detected as a function of the respective comparison result, and when an error is detected, the data are loaded into the cache memory in renewed fashion.

13. A device for error detection in a cache memory for storing data, the access to the data stored in the cache memory taking place by addresses assigned to them,
wherein means are included which for the addresses assigned to the stored data, generate at least one first test signature made up of at least one first signature bit and also store it in the cache memory.

14. The cache memory having a device for error detection, the access to the data stored in the cache memory taking place by addresses assigned to them,
wherein for the addresses assigned to the stored data, at least one first test signature made up of at least one first signature bit is generated and this first test signature is stored in the cache memory.